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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,752	12/30/2003	Matthew Mattina	42P17893	9070

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,752	MATTINA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 14 July 2005 has been fully considered by the Examiner.

Drawings

2. The drawings were received on 30 December 2003. These drawings are deemed acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bordaz et al., hereinafter Bordaz (US Patent 6,195,728 B1).

As for claim 1, Bordaz teaches a system for maintaining cache coherency in a CMP comprising:

one or more processor cores (Fig. 1, elements 11-14, 31-34, 51-54 and 71-74 depict a plurality of processor cores);

a shared cache (Fig. 1, memory (element 5) is shared among at least two processors));

and a ring, wherein the ring connects the one or more processors and the shared cache (Fig. 1, element 16 – the ring is used for communication between each module (elements 10, 20, etc) which each contain a plurality of processors;

As for claim 2, Bordaz teaches the system of claim 1 wherein the one or more processor cores each include a private cache (each processor contains its own private cache as depicted in Fig. 1 (element 11 is the private cache for processor 1 for example)).

As for claim 3, Bordaz teaches the system of claim 1 wherein shared cache includes one or more cache banks (inherently all cache memory must be arranged in a configuration of at least one bank. Additionally, Bordaz indicates that each shared cache contains a remote access cache (RC – element 15), which is a separate memory bank within the shared cache (element 5)).

As for claim 4, Bordaz teaches wherein the one or more cache banks is responsible for a subset of a physical address space of the system (col. 4, lines 28-46 – the RC (element 15) makes up a portion of the total physical memory of memory element 5).

As for claims 5 and 6, Bordaz teaches the system of claim 1 wherein the one or more processor cores are write-thru, which write data through to the shared cache (col. 7, lines 56-65 – Bordaz discusses a write through cache mechanism which writes to reserved zones in the shared cache (i.e. element 25)).

As for claim 10, Bordaz teaches the system of claim 1 wherein the one or more processor cores accesses data from the shared cache (col. 4, lines 47-53 – each processor accesses data blocks in the shared memories).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bordaz as applied to claim 1 above, and in further view of Fletcher (US Patent 4,445,174).

As for claims 7 through 9, though Bordaz teaches the system of claim 1, wherein the one or more processor cores include a buffer, he fails to teach the buffer as functioning merge buffer capable of purging stored data to a shared cache.

Fletcher however teaches a multiprocessor system including a shared cache which a processor's private cache (Fig. 1, element 8) continuously stores data (permitting the merging of data (i.e. line by line) into the private memory from the main memory until an eviction is requested) –col. 1, line 62-68, and then moves the lines directly from a private cache to the shared cache, while circumventing the system's main memory (col. 2, lines 56-64).

As for claim 11, Fletcher further discloses the private cache, which is used to merge data from the memory line by line, as coalescing multiple lines to a same block of the shared cache – col. 3, line 17-25 – copies of the same shared memory block may exist simultaneously in each private cache. In other words, data stored in a processor's private cache can exist as one memory block of the shared memory.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Bordaz to further include Fletcher's multiprocessor system including a shared cache to his own system. By doing so, Bordaz would benefit by improving system performance by having a means of automatically detecting lines of information moved to the shared cache, hence eliminating "pingponging" of lines between requesting processors as taught by Fletcher in col. 2, lines 49-65.

5. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bordaz as applied to claim 1 above, and in further view of Koenen (US PG Publication 2004/0019891 A1).

As for claims 12 and 13, though Bordaz teaches connecting his each processor module via a ring configuration as claimed by Applicant in claim 1, he fails to specifically teach the ring configuration as recited by Applicant in claims 12-13 of the pending Application.

Koenen however teaches an apparatus for optimizing performance in a multi-processing system, which includes connecting a plurality of module nodes

via a synchronous, unbuffered, bi-directional ring with a fixed deterministic latency as recited by Applicant in claim 12-13. Referring to Fig. 1, a plurality of processing nodes (elements 12, 14 and 16) are connected for bi-directional communication (elements 12J, 14J and 16J) with the interconnect fabric (element 18). Note Koenen describes the fabric as including a ring structure in paragraph 0019, lines 9-12. The ring functions without the aid of a buffering system (i.e. unbuffered), and supports synchronous connections with a minimum static latency around the ring (paragraph 0026, lines 7-12 – the minimum latency is static). Furthermore, paragraph 0023 (and subsequently Table 1), describe preset latencies between each node depending on the number of nodes included in the system. With this table, the overall latency of the entire ring interconnect is known (likewise, fixed), which allows the system to synchronize communication between nodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention, for Bordaz to implement Koenen's apparatus for optimizing performance in a multi-processing system. By doing so, Bordaz would benefit by using a superior interconnection fabric (as shown by Koenen in Fig. 1, element 18) for his processing modules, which in turn could help Bordaz's NUMA machine by reducing access latency and increase system performance as taught by Koenen in paragraph 0011, lines 1-15.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Oner et al. (US PG Publication 2005/0080953 A1) disclose a fragment storage for data alignment and merger which includes a storage buffer to merge data being transferred on a plurality of channels.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER